Mirror Technologies

*Reflecting Ideas..*

✓ ***100 % OUTPUT AND QUALITY ASSURANCE***

✓ ***100% PRACTICAL TRAINING ON ALL DOMAINS***

## *VLSI IEEE PROJECT TITLES LIST*

**TECHNONLOGY : VLSI**

**DOMAIN : IEEE TRANSACTIONS ON CORE VLSI**

| S.NO | CODE | TITLES |
|---|---|---|
| 1 | VLSIO01 | DESIGN OF CORDIC CORE ALGORITHM IN FPGA |
| 2 | VLSIO02 | DEVIATION-BASED LFSR RESEEDING FOR TEST-DATA COMPRESSION |
| 3 | VLSIO03 | NOVEL BCD ADDERS AND THEIR REVERSIBLE LOGIC IMPLEMENTATION FOR IEEE 754R FORMAT |
| 4 | VLSIO04 | AUTOMATIC CONSTRAINT BASED TEST GENERATION FOR BEHAVIORAL HDL MODELS |
| 5 | VLSIO05 | ARCHITECTURE FOR DYNAMIC DATA SCALING IN 2/4/8K PIPELINE FFT CORES |
| 6 | VLSIO06 | AN AREA-EFFICIENT UNIVERSAL CRYPTOGRAPHY PROCESSOR FOR SMART CARDS |
| 7 | VLSIO07 | DESIGN OF PIC MICROCONTROLLER IN FPGA |
| 8 | VLSIO08 | COMPACT HARDWARE DESIGN OF WHIRLPOOL HASHING CORE |
| 9 | VLSIO09 | DESIGN A LOW POWER BOOTH MULTIPLIER IN FPGA |
| 10 | VLSIO10 | UART MODULE FOR REAL TIME APPLICATION |

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| | | |
|---|---|---|
| 11 | VLSIO11 | DESIGN A HIGH SPEED FIRST-IN FIRST-OUT (FIFO) IN FPGA |
| 12 | VLSIO12 | IMPLEMENTING AND OPTIMIZING A DIRECT DIGITAL FREQUENCY SYNTHESIZER (DDFS) ON FPGA |
| 13 | VLSIO13 | IMPLEMENTATION OF PHASE SHIFT KEYING (QPSK, BPSK) |
| 14 | VLSIO14 | IMPLEMENTATIONS OF QUADRATURE AMPLITUDE MODULATION TECHNIQUE |
| 15 | VLSIO15 | HIGH SPEED FPGA ARCHITECTURES FOR THE DATA ENCRYPTION STANDARD |
| 16 | VLSIO16 | IMPLEMENTATION OF TINY ENCRYPTION ALGORITHM (TEA) |
| 17 | VLSIO17 | IMPLEMENTATION OF TWO FISH CRYPTOGRAPHIC ALGORITHM |
| 18 | VLSIO18 | SECURE HASH ALGORITHM (SHA) |
| 19 | VLSIO19 | RTL DESIGN AND SIMULATION OF MICRO-CONTROLLER IN HDL |
| 20 | VLSIO20 | DESIGN OF UART TRANSMITTER MODULE AND UART RECEIVER MODULE |
| 21 | VLSIO21 | DESIGN AND SIMULATION OF MEMORY BLOCKS OF RAM AND ROM IMPLEMENTATION IN VLSI |
| 22 | VLSIO22 | IMPLEMENTATION OF QUARTURE PHASE SHIFT KEYING (QPSK). |
| 23 | VLSIO23 | RADIX-2 FOR FLOATING POINT DIVISION |

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| | | |
|---|---|---|
| 24 | VLSIO24 | FREQUENCY HOPPING SPREAD SPECTRUM TECHNIQUE |
| 25 | VLSIO25 | QUADRATURE AMPLITUDE MODULATION TECHNIQUE |
| 26 | VLSIO26 | DESIGN OF FLOATING POINT ADDITION, SUBTRACTION AND MULTIPLICATION UNIT USING VHDL |
| 27 | VLSIO27 | DESIGN OF VITERBI DECODER |
| 28 | VLSIO28 | VHDL CODE FOR 3*3 MATRIX MULTIPLICATION |
| 29 | VLSIO29 | IMPLEMENTATION OF RJINDAEL ALGORITHM |
| 30 | VLSIO30 | FORWARD ERROR CORRECTION TECHNIQUE USING VITERBI ALGORITHM |
| 31 | VLSIO31 | DESIGN OF MANCHESTER ENCODER/DECODER USING VHDL |
| 32 | VLSIO32 | DIRECT SEQUENCE SPREAD SPECTRUM TECHNIQUE |
| 33 | VLSIO33 | IMPLEMENTATION OF MAC UNIT |
| 34 | VLSIO34 | DESIGN OF REVERSIBLE MULTIPLIER USING VHDL |
| 35 | VLSIO35 | UART WITH FIFO FOR SERIAL COMMUNICATION USING VHDL/VERILOG |
| 36 | VLSIO36 | DESIGN OF VEDIC MULTIPLIER USING VHDL |